| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments |
|---|---|---|---|---|---|---|---|
| 22 | BRS | L22 | 56 | (detect$4 or determin$4 or calculat$4) near4 (noise near2 error$1) with (compar$4) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:05 | |
| 23 | BRS | L23 | 76 | (detect$4 or determin$4 or calculat$4 or generat$4) near4 (noise near2 error$1) with (compar$4) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:21 | |
| 24 | BRS | L24 | 1377 | (high near2 compar$6 or upper near2 compar$6 or maxim$4 near2 compar$6 or Upper adj2 voltage or high$3 adj2 voltage or maxim$4 adj2 voltage or "Vmax") with (low near2 compar$4 or lower near2 compar$6 or minim$4 near2 compar$6 or "Vmin" or lower adj2 voltage or minim$4 adj2 voltage) same (clock$4) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:17 | |
| 25 | BRS | L25 | 1 | 23 and 24 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:10 | |
| 26 | BRS | L26 | 1 | 23 same (FF$1 or flip adj1 flop$1 or sampl$3 adj2 hold$3 or "S/H" or DFF$1 or D adj1 FF$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:12 | |

| | Error Definition | Errors |
|---|---|---|
| 22 | | |
| 23 | | |
| 24 | | |
| 25 | | |
| 26 | | |

| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments |
|---|---|---|---|---|---|---|---|
| 27 | BRS | L27 | 14 | 23 and(FF$1 or flip adj1 flop$1 or sampl$3 adj2 hold$3 or "S/H" or DFF$1 or D adj1 FF$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:12 | |
| 28 | BRS | L28 | 38543 | (high near2 compar$6 or upper near2 compar$6 or maxim$4 near2 compar$6 or Upper adj2 voltage or high$3 adj2 voltage or maxim$4 adj2 voltage or "Vmax") with (low near2 compar$4 or lower near2 compar$6 or minim$4 near2 compar$6 or "Vmin" or lower adj2 voltage or minim$4 adj2 voltage) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:16 | |
| 29 | BRS | L29 | 2 | 23 and 28 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:16 | |

| | Error Definition | Errors |
|---|---|---|
| 27 | | |
| 28 | | |
| 29 | | |

| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments |
|---|---|---|---|---|---|---|---|
| 30 | BRS | L30 | 918 | (high near2 compar$6 or upper near2 compar$6 or maxim$4 near2 compar$6 or Upper adj2 voltage or high$3 adj2 voltage or maxim$4 adj2 voltage or "Vmax") with (low near2 compar$4 or lower near2 compar$6 or minim$4 near2 compar$6 or "Vmin" or lower adj2 voltage or minim$4 adj2 voltage) same (FF$1 or flip adj1 flop$1 or sampl$3 adj2 hold$3 or "S/H" or DFF$1 or D adj1 FF$1 or shift$3 adj2 register$3) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:18 | |
| 31 | BRS | L31 | 0 | 23 and 30 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:19 | |
| 32 | BRS | L32 | 110 | (high adj2 compar$6 with high adj2 voltage$1) same (low adj2 compar$6 with low adj2 voltage$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:29 | |
| 33 | BRS | L33 | 0 | 23 and 32 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:21 | |

| | Error Definition | Errors |
|---|---|---|
| 30 | | |
| 31 | | |
| 32 | | |
| 33 | | |

| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments |
|---|---|---|---|---|---|---|---|
| 34 | BRS | L34 | 1774 | (detect$4 or determin$4 or calculat$4 or generat$4) near4 (noise near2 error$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:22 | |
| 35 | BRS | L35 | 0 | 32 and 34 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:22 | |
| 36 | BRS | L36 | 0 | 32 and (noise near2 error$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:23 | |
| 37 | BRS | L37 | 80 | (alarm$3 or flag$1 or beep$3) with (noise near2 error$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:24 | |
| 38 | BRS | L39 | 0 | 37 same (logic near2 sequenc$3 or sequencer$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:25 | |
| 39 | BRS | L38 | 1 | 37 same (logic near2 circuit$3 or logic near2 device$1 or combin$10 near2 sequenc$3 or combin$10 near2 circuit$3 or combin$10 near2 device$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:26 | |

| | Error Definition | Errors |
|---|---|---|
| 34 | | |
| 35 | | |
| 36 | | |
| 37 | | |
| 38 | | |
| 39 | | |

| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments |
|---|---|---|---|---|---|---|---|
| 40 | BRS | L40 | 27 | 37 and (logic near2 circuit$3 or logic near2 device$1 or combin$10 near2 sequenc$3 or combin$10 near2 circuit$3 or combin$10 near2 device$1 or sequencer or logic near3 sequenc$3) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:27 | |
| 41 | BRS | L41 | 0 | 32 and 40 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:27 | |
| 42 | BRS | L42 | 65973 | (high adj2 compar$6 or high adj2 voltage$1) same (low adj2 compar$6 or low adj2 voltage$1) | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:27 | |
| 43 | BRS | L43 | 0 | 42 and 40 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:28 | |
| 44 | BRS | L44 | 25 | ((JYH-MING) near2 (JONG)).INV. | US-PGPUB; USPAT; USOCR | 2006/06/23 20:28 | |
| 45 | BRS | L45 | 23 | ((LEO) near2 (YUAN)).INV. | US-PGPUB; USPAT; USOCR | 2006/06/23 20:28 | |

| | Error Definition | Errors |
|---|---|---|
| 40 | | |
| 41 | | |
| 42 | | |
| 43 | | |
| 44 | | |
| 45 | | |

| | Type | L # | Hits | Search Text | DBs | Time Stamp | Comments |
|---|---|---|---|---|---|---|---|
| 46 | BRS | L46 | 34 | 44 or 45 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:28 | |
| 47 | BRS | L47 | 6 | (high adj2 compar$6 or high adj2 voltage$1) and 46 | US-PGPUB; USPAT; EPO; JPO | 2006/06/23 20:29 | |

| | Error Definition | Errors |
|---|---|---|
| 46 | | |
| 47 | | |

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## Inventor Name Search Result

Your Search was:

Last Name = JONG
First Name = JYH-MING

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 09698622 | Not Issued | 71 | 10/27/2000 | Noise margin self-diagnostic receiver logic | JONG, JYH-MING |
| 09707191 | 6504486 | 150 | 11/06/2000 | DUAL VOLTAGE SENSE CELL FOR INPUT/OUTPUT DYNAMIC TERMINATION LOGIC | JONG, JYH-MING |
| 09741485 | 6737892 | 150 | 12/18/2000 | METHOD AND APPARATUS FOR DETECTING VALID CLOCK SIGNALS AT A CLOCK RECEIVER CIRCUIT | JONG, JYH-MING |
| 09797033 | 6404839 | 150 | 02/28/2001 | SELECTABLE CLOCK DIVIDER CIRCUIT WITH A 50% DUTY CYCLE CLOCK | JONG, JYH-MING |
| 09842332 | 6937680 | 150 | 04/24/2001 | SOURCE SYNCHRONOUS RECEIVER LINK INITIALIZATION AND INPUT FLOATING CONTROL BY CLOCK DETECTION AND DLL LOCK DETECTION | JONG, JYH-MING |
| 09879501 | 6518792 | 150 | 06/11/2001 | METHOD AND CIRCUITRY FOR A PRE-EMPHASIS SCHEME FOR SINGLE-ENDED CENTER TAPED TERMINATED HIGH SPEED DIGITAL SIGNALING | JONG, JYH-MING |
| 09929150 | Not Issued | 161 | 08/13/2001 | Optical receiver for receiving a plurality of input signals | JONG, JYH-MING |
| 09929153 | 7039323 | 150 | 08/13/2001 | OPTICAL TRANSMITTER FOR TRANSMITTING A PLURALITY OF OUTPUT SIGNALS | JONG, JYH-MING |
| 09931696 | 6542026 | 150 | 08/15/2001 | APPARATUS FOR ON-CHIP REFERENCE VOLTAGE GENERATOR FOR RECEIVERS | JONG, JYH-MING |

| | | | | | |
|---|---|---|---|---|---|
| | | | | IN HIGH SPEED SINGLE-ENDED DATA LINK | |
| 09951928 | 6944692 | 150 | 09/13/2001 | AUTOMATED CALIBRATION OF I/O OVER A MULTI-VARIABLE EYE WINDOW | JONG, JYH-MING |
| 09952951 | 6512704 | 150 | 09/14/2001 | DATA STROBE RECEIVER | JONG, JYH-MING |
| 09999877 | 6880118 | 150 | 10/25/2001 | SYSTEM AND METHOD FOR TESTING OPERATIONAL TRANSMISSIONS OF AN INTEGRATED CIRCUIT | JONG, JYH-MING |
| 10027544 | 6690191 | 150 | 12/21/2001 | BI-DIRECTIONAL OUTPUT BUFFER | JONG, JYH-MING |
| 10117427 | Not Issued | 71 | 04/05/2002 | Source synchronous bus repeater | JONG, JYH-MING |
| 10625298 | 6853594 | 150 | 07/22/2003 | DOUBLE DATA RATE (DDR) DATA STROBE RECEIVER | JONG, JYH-MING |
| 10626228 | Not Issued | 30 | 07/24/2003 | Source synchronous I/O bus retimer | JONG, JYH-MING |
| 10977214 | Not Issued | 20 | 10/29/2004 | Dynamically configurable symmetric multi-processors | JONG, JYH-MING |
| 11224277 | Not Issued | 30 | 09/12/2005 | Automated calibration of I/O over a multi-variable eye window | JONG, JYH-MING |
| 60455311 | Not Issued | 159 | 03/17/2003 | Circuit and method employing signal emphasis for high-speed communication | JONG, JYH-MING |

## Inventor Search Completed: No Records to Display.

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## Inventor Name Search Result

Your Search was:

Last Name = YUAN
First Name = LEO

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 06468262 | Not Issued | 161 | 02/22/1983 | INTERCONNECTION CHANGE PAD FOR USE IN CHANGING THE INTERCONNECTION PATTERN OF AN INTEGRATED CIRCUIT MOUNTING SUBSTRATE | YUAN, LEO |
| 06565318 | 4553050 | 150 | 12/27/1983 | TRANSMISSION LINE TERMINATOR-DECOUPLING CAPACITOR CHIP FOR OFF-CHIP DRIVER | YUAN, LEO |
| 06591342 | 4597029 | 150 | 03/19/1984 | SIGNAL CONNECTION SYSTEM FOR SEMICONDUCTOR CHIP | YUAN, LEO |
| 08640096 | 6310489 | 150 | 04/30/1996 | METHOD TO REDUCE WIRE-OR GLITCH IN HIGH PERFORMANCE BUS DESIGN TO IMPROVE BUS PERFORMANCE | YUAN, LEO |
| 08763687 | 6239619 | 150 | 12/11/1996 | METHOD AND APPARATUS FOR DYNAMIC TERMINATION LOGIC OF DATA BUSES | YUAN, LEO |
| 09320794 | 6516422 | 150 | 05/27/1999 | COMPUTER SYSTEM INCLUDING MULTIPLE CLOCK SOURCES AND FAILOVER SWITCHING | YUAN, LEO |
| 09324399 | 6477205 | 150 | 06/03/1999 | DIGITAL DATA TRANSMISSION VIA MULTI-VALUED LOGIC SIGNALS GENERATED USING MULTIPLE DRIVE STATES EACH CAUSING A DIFFERENT AMOUNT OF CURRENT TO FLOW THROUGH A TERMINATION RESISTOR | YUAN, LEO |

| | | | | | |
|---|---|---|---|---|---|
| 09698622 | Not Issued | 71 | 10/27/2000 | Noise margin self-diagnostic receiver logic | YUAN, LEO |
| 09707191 | 6504486 | 150 | 11/06/2000 | DUAL VOLTAGE SENSE CELL FOR INPUT/OUTPUT DYNAMIC TERMINATION LOGIC | YUAN, LEO |
| 09741485 | 6737892 | 150 | 12/18/2000 | METHOD AND APPARATUS FOR DETECTING VALID CLOCK SIGNALS AT A CLOCK RECEIVER CIRCUIT | YUAN, LEO |
| 09842332 | 6937680 | 150 | 04/24/2001 | SOURCE SYNCHRONOUS RECEIVER LINK INITIALIZATION AND INPUT FLOATING CONTROL BY CLOCK DETECTION AND DLL LOCK DETECTION | YUAN, LEO |
| 09879501 | 6518792 | 150 | 06/11/2001 | METHOD AND CIRCUITRY FOR A PRE-EMPHASIS SCHEME FOR SINGLE-ENDED CENTER TAPED TERMINATED HIGH SPEED DIGITAL SIGNALING | YUAN, LEO |
| 09931696 | 6542026 | 150 | 08/15/2001 | APPARATUS FOR ON-CHIP REFERENCE VOLTAGE GENERATOR FOR RECEIVERS IN HIGH SPEED SINGLE-ENDED DATA LINK | YUAN, LEO |
| 09951928 | 6944692 | 150 | 09/13/2001 | AUTOMATED CALIBRATION OF I/O OVER A MULTI-VARIABLE EYE WINDOW | YUAN, LEO |
| 09999877 | 6880118 | 150 | 10/25/2001 | SYSTEM AND METHOD FOR TESTING OPERATIONAL TRANSMISSIONS OF AN INTEGRATED CIRCUIT | YUAN, LEO |
| 11224277 | Not Issued | 30 | 09/12/2005 | Automated calibration of I/O over a multi-variable eye window | YUAN, LEO |
| 60013477 | Not Issued | 159 | 03/15/1996 | METHOD AND APPARATUS IMPLEMENTING A SPLIT TRANSACTION SNOOPING BUS, SNOOPING ON A SPLIT TRANSACTION BUS, EXTENDING THE COHERENCE DOMAIN BEYOND A BUS, OPTIMIZING GLOBAL DATA REPLIES, ARBITRATING FOR ACCESS TO A SHARED RESOURCE, AND PROVIDING | YUAN, LEO |

| | | | | | |
|---|---|---|---|---|---|
| | | | | SHORT LATENCY PRIORITIZED ROUND-RO | |
| 10325233 | Not Issued | 95 | 12/19/2002 | APPARATUS AND PROCESS FOR CONTINUOUS SOLID-STATE POLY-CONDENSATION IN A FLUIDIZED REACTOR WITH MULTIPLE STAGES | YUAN, LEON |
| 10750292 | Not Issued | 30 | 12/31/2003 | Regeneration method with efficient oxygen utilization | YUAN, LEON |
| 11015156 | Not Issued | 20 | 12/17/2004 | Multi-catalyst selection for chlorided reforming catalyst | YUAN, LEON |

## Inventor Search Completed: No Records to Display.

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